AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Original): A management system for a dynamic random access memory (DRAM) module socket, the management system comprising:

a basic input/output system (BIOS) for storing an access control program and outputting a control signal when the access control program is activated;

a chipset comprising a pair of general purpose input/output (GPIO) terminals and a pair of access control mode output ports, the chipset connected to the BIOS for receiving the control signal and correspondingly outputting a first control output and a second control output respectively via the GPIO terminals, and outputting a first access control signal and a second access control signal respectively via the access control mode output ports;

a dynamic random access memory (DRAM) module socket comprising three access control mode input ports; and

a pair of switches for respectively receiving the first access control signal and the second access control signal and selectively outputting the first access control signal and the second access control signal to the three access control mode input ports respectively according to the first control output and the second control output.

Claim 2 (Original): The management system of claim 1, wherein the chipset is an integrated chipset.

Claim 3 (Original): The management system of claim 1, wherein the pair of access control mode output ports are an Error Correction Code (ECC)/Clock Enable (CKE) mode output port and a Data Input Output Mask (DQM)/CKE mode output port.

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Claim 4 (Currently Amended): The ~~managing~~ management system of claim 1, wherein the DRAM module socket is a DDRDRAM socket.

Claim 5 (Currently Amended): The ~~managing~~ management system of claim 1, wherein the DRAM module socket is a RDRAM socket.

Claim 6 (Currently Amended): The ~~managing~~ management system of claim 1, wherein the three access control mode input ports are an ECC mode input port, a CKE mode input port and a DQM mode input port.

Claim 7 (Currently Amended): The ~~managing~~ management system of claim 1, wherein the switches respectively receive the first control output and the second control output to selectively output the first access control signal and the second access control to two of the three access control mode input ports.

Claim 8 (New): A management system for a dynamic random access memory (DRAM) module socket, the management system comprising:

a basic input/output system (BIOS) comprising an access control program, the BIOS outputting a control signal when the access control program is activated;

a chipset comprising a first and second general purpose input/output (GPIO) terminal and a first and second access control mode output port, the chipset connected to the BIOS for receiving the control signal and correspondingly outputting a first control output signal via the first GPIO terminal, a second control output signal via the second GPIO terminal, a first access control signal via the first access control mode output port, and a second access control signal via the second access control mode output port;

a dynamic random access memory (DRAM) module socket comprising a first, second, and third access control mode input port;

a first switch comprising a first input connected to the first access control mode output port, a first output electrically connected to the first access control

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mode input port, a second output electrically connected to the second access control mode input port, and a control terminal electrically connected to the first GPIO terminal for outputting the first access control signal selectively to the first or to the second access control mode input port according to the first control output signal; and

a second switch comprising a first input connected to the second access control mode output port, a first output electrically connected to the second access control mode input port, a second output electrically connected to the third access control mode input port, and a control terminal electrically connected to the second GPIO terminal for outputting the second access control signal selectively to the second or to the third access control mode input port according to the second control output signal.

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